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(54) Title A high speed ISDN terminal adapter for a standard modem interface

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A HIGH-SPEED ISDN TERMINAL ADAPTER FOR A STANDARD MODEM INTERFACE

The present invention relates to a high speed ISDN terminal adapter for a standard modem interface, for example allowing users of personal computers (PCs) to upgrade from a standard Hayes-compatible modem interface to the much faster ISDN interface, preferably with an inexpensive adapter embodied as an internal PC card connected to a PC communications port.

ISDN (Integrated Services Digital Network) is an international high-speed telecommunications network based on existing telephone lines and computer networks designed to handle video, text, voice, data, fax and graphic images which has been under development since 1985 by the International Telecommunications Union and multinational companies, and began to come into widespread use in the early 1990s. All signals created by a user terminal are transmitted over a single subscriber access line in digital form. An important aspect of the integration of services is the development of a standard set of user interfaces. However, while there is a very comprehensive set of CCITT standards (e.g. ISDN Layer 1, Q921, Q931) at the network level, there is still little or no real standardisation at the user interface level, or at least no internationally-accepted standard has emerged. This is in contrast to the more mature technology of modems, where a public domain user interface standard has come to exist, known under the generic name of Hayes Commands. It is difficult to know which ISDN user interface standard will predominate in future - for example, in the U.S.A., there is the WAN-MINI PORT standard, in Germany the CAPI standard, in France the COM-APPLI standard, etc., but for some time it will be necessary to provide PC users with support for "legacy applications" which were designed with Hayes Commands for communication via a standard modem, once they have upgraded to ISDN.

An ISDN Basic Rate data line is comprised of two B-channels and one D-channel. The B-channel is a communication channel used to support the transmission of say voice and/or image data (e.g. for videoconferencing) with a capacity of 64 Kbits/sec. The D-channel offers the lowest bit rate at 16 Kbits/sec. and may be used as a signalling channel for establishing B-channel links. For very high speed data/video transfer, the H12-channel operates at 1.92 Mbits/sec. Compared to a modem bit rate of 28.8 Kbits/sec, which is unlikely to be greatly exceeded due to commonly-encountered bandwith constraints, ISDN offers a very much faster system for digital information transfer.

ISDN standard user or application interfaces developed so far are characterised by

- being operating system-specific, and /or
- being a software interface as opposed to a purely hardware interface, or
- being a high speed physical interface such as a fibre optic interface (FIFO), shared memory, or direct memory access (DMA).

In general the bandwith of these interfaces is high compared to the bandwith of a standard modem interface. This results in complex input/output hardware. A problem is that the low level driver tends to be vendor-specific, allowing access to the user interface only through software, but as yet no de facto software standard has emerged. In contrast, all modems not only follow a software standard (Hayes Commands) and are compatible across all operating systems, but also follow a hardware standard since all designs are based on the 8250 or 16c550 universal asynchronous receiver transmitter (UART) derivatives. The disadvantage of the modem approach to digital information transfer is that the physical interface is based on a hardware component, or UART, which is inherently slow compared to ISDN line speeds, and which dates back to when UARTs were required to run at bit rates of 2.4 to 19.2 Kbits/sec. If this speed limitation of the UART could be overcome, it would still be a good solution for an ISDN adapter running at aggregate bit rates of 128 Kbits/sec.

Although solutions do exist allowing a synchronous data flow to be interfaced to the ISDN network using the V110, V120 and V14 standards, these standards deal mainly with encoding asynchronous data and line status information in a synchronous ISDN (V110/V120) frame, and do not address raw data rate across a UART interface. The standard prior art configuration for a UART implementation providing a user interface between an asynchonous user application and a synchronous ISDN "data pump" is shown in Figure 1 of the accompanying drawings. This will be referred to again below, but the basic configuration comprises a host UART and an application UART in a back-to-back arrangement with a low-speed serial interconnection, and suffers from the following disadvantages:

(a) it requires a crossover of configuration status and data in the serial interconnection; for example, request to send (RTS) at the host UART is connected to clear to send (CTS) at the applications or add-on UART, and clear to send (CTS) at the host UART is connected to request to send (RTS) at the applications UART. This is a null modem configuration in effect, and suffers from the inherent problem of not being efficiently able to signal line error conditions; for example to detect loss of carrier independently of data set ready (DSR);

(b) data transfer rate is limited by virtue of conversion of parallel data input/output across the host side to serial data transfer between the back-to-back UARTs, and reconversion back to parallel data transfer at the add-on side where an add-on processor decodes the Hayes signalling Commands and establishes the correct ISDN call. The whole process of serialisation, a required feature of modem communications, thus becomes an unwanted overhead which eventually limits data transfer rate;

(c) the parallel host side of the interface is underutilised because it is potentially capable of supplying data at megabit speeds as opposed to the kilobit speeds of a UART;

(d) when two ISDN B-channels are used allowing for two separate calls to be made at the same time on the same line, two back-to-back pairs of host and add-on UARTs are required, increasing parts count.

The present invention seeks to overcome the disadvantages of the prior art and to provide a high speed ISDN terminal adapter for a standard modem interface which preferably and advantageously

- provides hardware compatibility with standard UART chips used in PCs,
- is more efficient, for example in signalling line error conditions,
- maps all modem control signals to the correct ISDN signalling states,
- is of relatively low cost with a low parts count, provides a high-speed parallel data path (for example 8-bit, or 16-bit or 32 bit) without any intermediate serial interface, and
- maps Hayes Commands to ISDN call establishment procedures.

According to the present invention there is provided a high-speed ISDN terminal adapter for a standard modem interface which is capable of transferring digitally-encoded data input/output from a synchronous ISDN data pump to an asynchronous application resident in a host computer, wherein the adapter comprises interface means whereby the host application recognises the ISDN data pump as a standard UART interface and consists of a set of read-write line data registers, a set of control registers, and a set of status registers, and means to map said registers to an ISDN environment and to read/write said registers from the host computer side, an add-on processor adapted to directly read/write the line data registers, and a high speed parallel data pathway between the ISDN data pump and said interface means.

Advantageously, the interface means comprises an asynchronous communications port emulator (ACPE) comprising the following internal registers

- line data registers, write
- line data registers, read
- line control registers, write
- modem control registers, write
- line status registers, read
- modem status registers, read
- interrupt registers

wherein said registers may be read/written from/to either side of said interface.

Preferably the ACPE is adapted to work on an adapter card also comprising oth r components including the add-on processor.

The host interface advantageously emulates a standard 8250/16c550 UART, wherein the add-on processor, preferably a 80188 microprocessor, reads/writes all the ACPE internal registers including communication of line status and interrupt information directly to the host computer central processing unit in order to thereby emulate the behaviour of a UART.

The ACPE thus provides a means of interfacing standard asynchronous modem applications to an ISDN back end data pump.

Advantageously, the use of only parallel data pathways without a serial conversion saves on gate parts, and allows bit rates of up to 2M bits/sec to be measured between the host computer central processing unit and the add-on processor, and an aggregate ISDN Basic Rate data line speed of 128K bits/sec. (2 x 64K bits/sec)

A preferred embodiment of the invention will now be described in further detail with reference to the accompanying drawings, in which:

Figure 1 shows schematically a PRIOR ART configuration for a UART implementation providing a user interface between an asynchronous user application resident in a host computer and a synchronous ISDN data pump,

Figure 2 shows schematically a comparable configuration according to a preferred embodiment of the present invention,

Figure 3 is a register model of a standard UART, and

Figure 4 shows schematically the internal register organisation of the ACPE part of the configuration of the embodiment of the present invention shown in Figure 2.

Firstly, with reference to the PRIOR ART solution shown in Figure 1, the add on application requires two UARTS wired back to back with each other. The ISDN data pump 1 receives data from the UART pair 2,3 and inserts it into ISDN synchronous frames. In this configuration status and data are crossed over as follows;

HOST UART	APPLICATION UART	
TX	TX	;Transmit data.
RX	TX	;Receive data.
DTR	DSR,DCD	;Data Terminal Ready.
DSR,DCD	DTR	;Data Set Ready.
RTS	CTS	;Clear To Send.
CTS	RTS	;Request To Send.

This is a null modem configuration which is the standard method of writing two UARTs together which are not connected through a network, but suffers from the inherent problem of not being able to signal efficiently line error conditions such as loss of carrier independently of DSR.

Data I/O is parallel across the HOST interface, within the two UARTS data is serialised and then reconverted back to parallel data where the add-on processor decodes the Hayes signalling commands (ATxxxx) and establishes the correct ISDN call. The whole process of serialisation which was a required feature of modem communications becomes an unnecessary overhead and eventually limits the Data Transfer Rate in the above configuration.

The parallel host interface is a much faster interface and is potentially capable of supplying data at MegaBit speeds compared to the KiloBit speeds of a UART.

The use of two B channels requires two host UARTs back to back with two add-on UARTS.

Figure 2 shows an alternative solution in accordance with the present invention, where the back to back UARTs have been replaced using a single ACPE chip 4. The ACPE also has an added advantage of incorporating decode logic, a simple set of select signals (sel0,sel1) to map the ACPE to the standard host COM port settings.

HARDWARE COMPATABILITY

In order to provide hardware compatability the host application must see the ISDN interface as a standard UART interface. The UART interface consists of a set of data registers and a set of control and status registers. The use of these registers in a standard UART/MODEM configuration must now be mapped on to an ISDN environment. The host UART application will set up a set of control registers, these registers are for the main to assure compatability with the standard UART interface and have no operational use except for certain signals as outlined below.

The ACPE provides a compatible set of registers as shown in Figure 3 which is a register model of a standard 8250 UART chip.

The ACPE is designed to work on an intelligent ISDN card where the host interface is seen as standard 8250/16c550 UART and the add-on intelligent processor reads/writes the ACPE internal registers in order to emulate the behaviour of UART.

The ACPE contains registers that can be read and written from the host side as well as registers that can be read/written from the add-on side. The host side writes the LCR register to send Line control information to the add-on processor. The add-on processor writes the LSR in order send line status information to the host processor. Data is exchanged across the set of read/write LDR registers. The ISR register is written to by the add-on processor in order to generate and interpret to the host processor. The following registers are supported in the ACPE and are mapped to ISDN signalling/line states

LINE CONTROL registers	(LCR),	
LINE STATUS registers	(LSR),	
MODEM CONTROL registers	(MCR),	
MODEM STATUS registers	(MSR),	
BAUD-RATE registers	(BRG),	Not applicable.
LINE-DATA registers	(LDR),	
Interrupt registers	(ISR).	

In the ACPE register set the following bits have the following special function,

MSR bits.

MCR.DTR	When written as 0, clear any ISDN in progress.
MCR.RTS	Not used.

MSR bits.

MSR.DCD	When read as 0, the ISDN call has been cleared. When read as 1, the ISDN call is in progress.
MSR.CTS	Always active.
MSR.RI	Not used.
MCR.DSR	Always active (0)
MCR.DDTR	Not used.
MSR.DDCD	Not used.
MSR.DCTS	Not used.
MSR.DRI	Not used.

LSR bits.

LSR.DR	When read as 1, register LDR contains data read from the ISDN line.
LSR.THRE	When read as 1, register LDR is empty and may be written to so that data is sent to the ISDN line.
LSR.TEMT	When read as 1, register LDR is empty and may be written to so that data is sent to the ISDN line.
LSR.OE	Not used.

LSR.PE	Not used.
LSR.FE	Not used.
LSR.BI	Not used.

In addition a change in status of any of the above bits will generate an interrupt to the host CPU, the host interrupt will be reset upon reading the ISR registers and or reading/writing the LDR registers if the ISR.RX or ISR.TX bits were the source of the interrupt.

LOW parts count

The ACPE can be implemented in a single MACH 120 device. The pinout description of this device is as shown in Table I. This MACH 120 device replaces up to three costly devices in an equivalent ISDN/UART design (2xHigh Speed UART, Decode). The added benefit being a high speed parallel interface instead of a slow parallel to serial, serial to parallel interface. The relative cost gain is 4:1 using the MACH 120 ACPE approach instead of the back to back UART approach.

Parallel 1/0

The ACPE approach does not use any parallel to serial conversion thus saving on internal ACPE gate count. The use of parallel only back to back registers allows speeds of up to 2Mbits/sec to be measured between the host CPU and the add-on CPU.

Hayes Command to ISDN mapping

The standard call establishment commands are intercepted by the add-on CPU and are mapped to the internal ISDN applications program interface (API). The following mapping applies;

```
ATDnnnnnnnnn          ; ISDNcall(nnnnnnnnnn)
ATAnnnnnnnnn          ; ISDNaccept(accept incoming call nnnnnnnn)
ATSO=1                ; ISDNaccept(accept all incoming call)
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The following return codes apply;

CONNECT	; ISDN call OK (DCD bit is set to one)
NO CARRIER	; ISDN call NOK (DCD bit is set to zero)
NO CARRIER	; Call is torn down if DTR is set inactive.

Other standard HAYES return codes are supported for the sake of compatability with existing applications.

Conclusion

The ACPE is a high performance solution for supporting standard asynchronous applications across ISDN. The novelty of the solution resides in the fact that the internal register map of a standard UART is maintained with respect to a host CPU, whilst an add-on CPU can directly read/write data registers using high speed parallel I/O. Line status information is accessed by the host and add-on processors using the same parallel method. One/two of four PC communication (COM) ports can be configured using the COMSEL(x) configuration lines. The COM port base address is decoded internally according to the value of the COMSEL(x) lines. Multiple host COM ports can be emulated with the same physical ACPE device using internal address decode to select between the emulated COM port.

CLAIMS

1. A high-speed ISDN terminal adapter for a standard modem interface which is capable of transferring digitally-encoded data input/output from a synchronous ISDN data pump to an asynchronous application resident in a host computer, wherein the adapter comprises interface means (4) whereby the host application recognises the ISDN data pump (5) as a standard UART interface and consists of a set of read-write line data registers, a set of control registers, and a set of status registers, and means to map said registers to an ISDN environment and to read/write said registers from the host computer side, an add-on processor adapted to directly read/write the line data registers, and a high speed parallel data pathway between the ISDN data pump and said interface means.

2. An ISDN terminal adapter according to claim 1, wherein the interface means (4) comprises an asynchronous communications port emulator (ACPE) comprising the following internal registers

- line data registers, write
- line data registers, read
- line control registers, write
- modem control registers, write
- line status registers, read
- modem status registers, read
- interrupt registers

wherein said registers may be read/written from/to either side of said interface.

3. An ISDN terminal adapter according to claim 2, wherein the ACPE is adapted to work on an adapter card also comprising other components including the add-on processor.

4. An ISDN terminal adapter according to claim 2 or claim 3, wherein the host interface emulates a standard 8250/16c550 UART, wherein the add-on processor, preferably a 80188 microprocessor, reads/writes all the ACPE internal registers including communication of line status and interrupt information directly to the host computer central processing unit in order to thereby emulate the behaviour of a UART.

5. An ISDN terminal adapter according to any of the preceding claims and substantially as described herein with reference to and as shown in the accompanying drawings.

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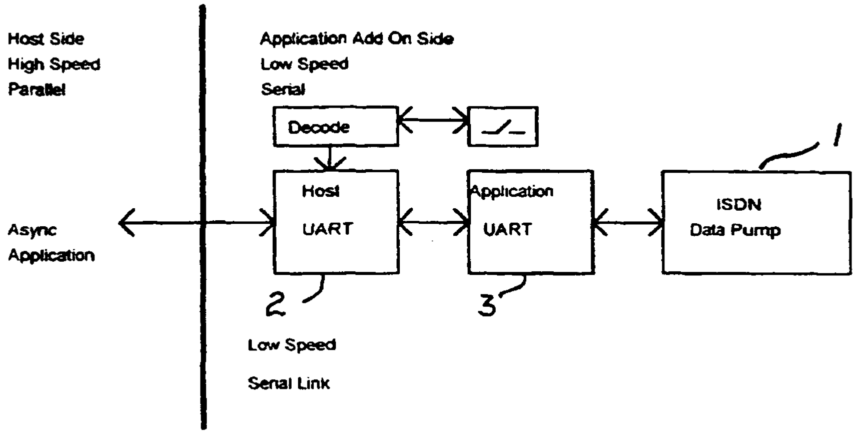

FIG. 1

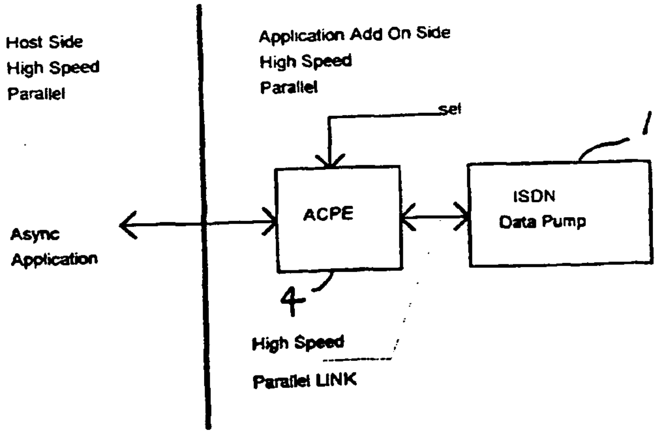

FIG. 2

base+0	data	LDR
base+1	Interrupt En.	IER
base+2	Interrupt Ident.	IER
base+3	Line Control	LCR
base+4	Modem Control	MCR
base+5	Line Status	LSR
base+6	Modem Status	MSR

FIG. 3

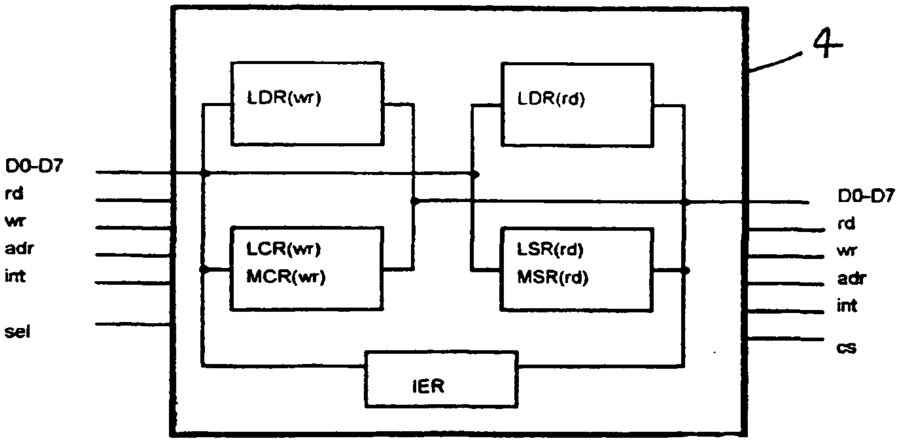

FIG. 4